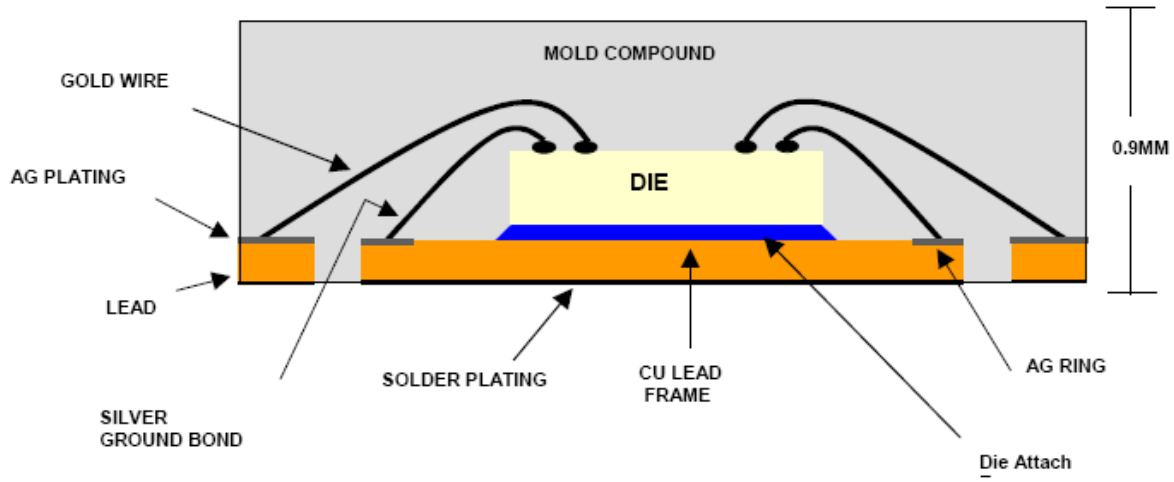
QFN Surface Mount Packages

Introduction

DigiMiMIc has chosen a low-cost, highperformance, surface mount package for delivery in volume of standard product lines for high-volume digital and analog applications. The package is the industry standard (JEDEC) known as the QFN (MO-220) package (Quad Flat No Leads). Originally intended for low-speed, high-density electronic components (op-amps, low-speed UARTs, CMOS converters, and cell phones) DigiMiMIc has been able to expand the capability of this technology using its IC expertise to extend RF and digital performance beyond 15 GHz.

Package Description

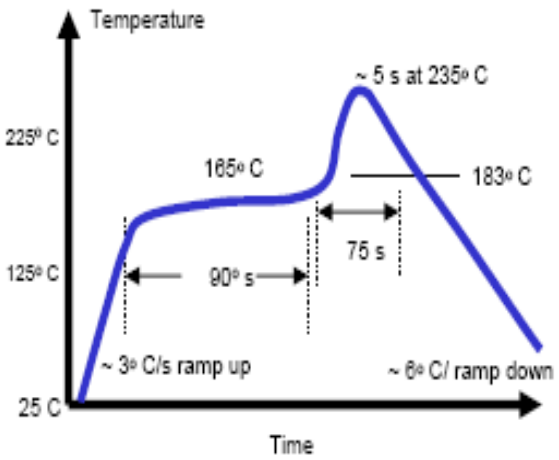
The cross section of a typical package below shows baseline construction of an IC mounted in the package. The package consists of a copper lead frame for excellent thermal properties with epoxy die-mounted ICs, gold wire bonds, and transfer molded epoxy resin sealed encapsulation.

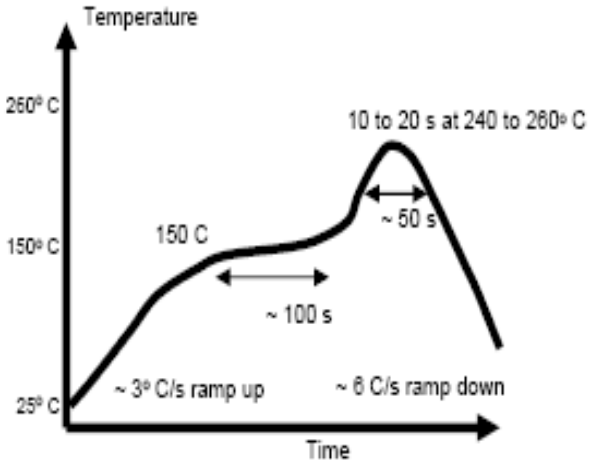


Production Pick-and-Place, Temperature Reflow

The 4 x 4 mm QFN package can be picked and placed by standard production handling equipment for surface mount devices. The parts are shipped in ESD safe plastic tubes. Temperature profiles for convection and IR reflow are as follows:

1. For 63/37 eutectic solder, temperature shall not exceed 240o C with time above liquidus temperature (183o C) of 60 to 150 s
2. For lead-free solder, the reflow temperature shall not exceed 260o C with time aboveliquidus temperature (217o C) of 60 to 150 s





Digimimic
via dell'Orsa Maggiore 21, 00144 Rome, Italy
Phone +39 (06) 5582904
FAX +39 (06) 5587394

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PCB Pattern and Layout

Prior to assembly, PCBs shall meet the solderability requirements of ANSI/J-STD-003 and be flat to within 0.1 mm per linear centimeter. The design requirements shall meet IPC-D-275. Surface geometry guidelines for layout are the following:

• Plated through holes or vias in the PCB lands for the package terminal connections are not allowed.
• Thermal vias should be used on a large thermal pad to improve thermal performance. The number of vias depends on package power dissipation and total PCB construction/ground plane design.
• The solder mask opening dimensions are should be as tight as possible to ensure some solder mask remains between PCB pads, preventing shorts during reflow.
• Solder mask misregistration shall not reduce the effective length or width of the PCB pad by more than 0.002 in. (0.05 mm).
• No residues (eg. undeveloped resist) shall be visible on solder pads at 7x magnification.
• The solder mask opening should be at least 0.0025 in. (0.064 mm) inward from the edge of the PCB thermal pad.
• There should be a minimum clearance of 0.006 in. (0.152 mm) between the edges of the PCB and the land patterns to avoid shorts.

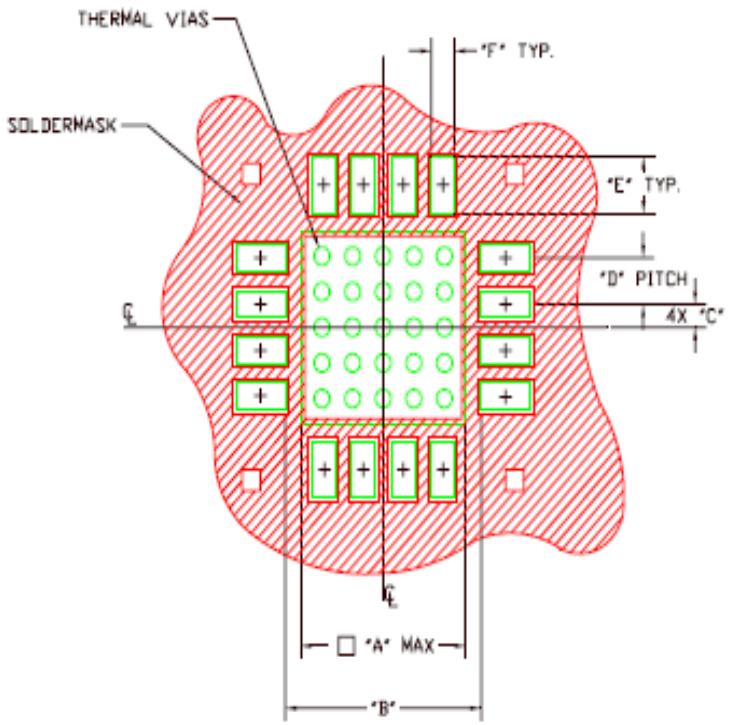
Recommended PCB layout

The PCB layout at right applies to both ROHS and non-ROHS QFN packages from DigiMiMIc.

It allows ROHS and non-ROHS parts to be used without PCB layout changes.

PCB fabrication tolerance = 0.002 in. (0.05 mm).

Package placement tolerance
= 0.002 in. (0.05mm).



Package size	Number of leads	Dimensions (mm)					
		A	B	C	D	E	F
4x4	16	2.59	3.20	0.325	0.650	0.80	0.38
5X5	20	3.59	4.20	0.325	0.650	0.80	0.38

Package size	Number of leads	Dimensions (in.)					
		A	B	C	D	E	F
4x4	16	0.102	0.126	0.013	0.026	0.031	0.015
5X5	20	0.141	0.165	0.013	0.026	0.031	0.015

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Package Storage/ Moisture Sensitivity

The following guidelines apply to the QFN (MO-220) 4 x 4 or 5 x 5 mm packages:

- Packages are classified as MSL-3 for storage and shelf life before reflow and production use.
- MSL-3 allows 168 hr. shelf life at <30o C, <60% relative humidity.
- With these conditions, there is no pre-baking required before solder reflow. Parts should bekept in dry packs prior to use.

RF Design Guidelines

The following guidelines apply to the QFN (MO-220) 4 x 4 or 5 x 5 mm packages:

- Input and output RF lines designed in microstrip are recommended at 50-ohm nominal impedance.
- Typical microstrip lines should be designed for 50 ohms at nominal trace widths of 0.015 in., making compatible traces to QFN pads.
- The use of top layer dielectric low-loss materials is recommended.
- Material such as Rogers 4000 series commercial low loss may be utilized. See the following link: http://www.rogerscorporation.com/acm/litintbl.htm#Product%20Data%20Sheets. As an example, Rogers R-4350 material with a dielectric constant of 3.48 and layer thickness of 0.004 in. will yield a trace width of 0.009 in. Rogers R4003 with a dielectric constant of 3.38 and thickness of 0.008 in. will yield a 50-ohm line at 0.017 in. trace width.
- FR-4 designs with dielectric constant of 4.6 would require a 0.008 in. top layer thickness, with 0.5 oz. copper cladding, microstrip top side, and full ground plane on bottom side. This will allow 0.014 in. microstrip line for routing of RF traces to the QFN package.

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