DM7080
12.5 Gb/s Wideband D Flip-Flop
(Advanced Information)

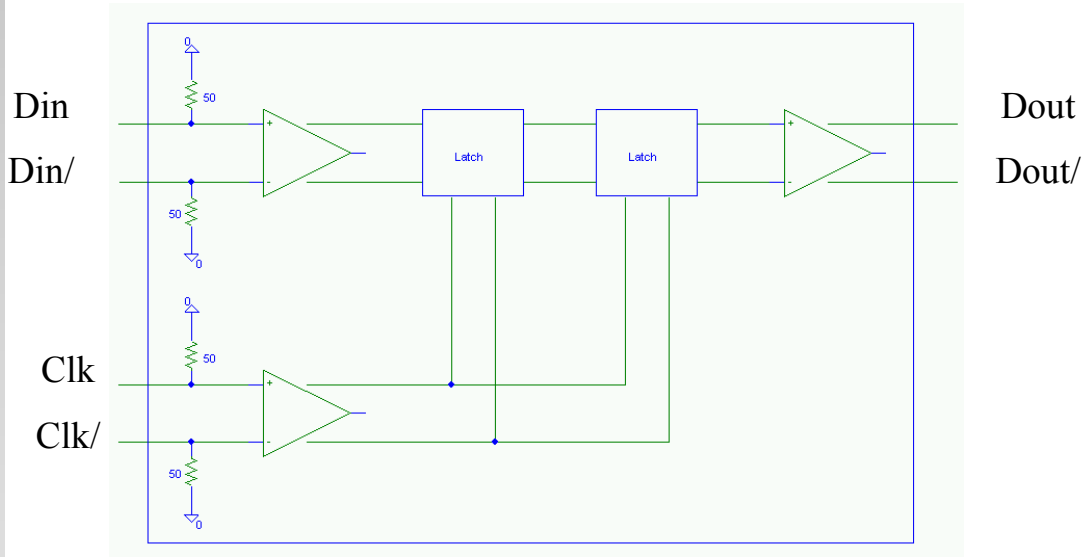
Description

The DM7080 is a high-speed D-type flip flop fabricated using 1-µm HBT GaAs technology. Its high output voltage, excellent rise and fall time and the high eye diagram quality at all clock frequencies makes the DM7080 suitable for very high speed and complex digital applications such as decision circuits, waveform shaping, register implementation, and timing adjustment. The device consists of a master-slave latch designed using an ECL topology guarantee high-speed operation. The data and clock inputs and data outputs are DC coupled. At the data input port, the DM7080 tolerates a wide range of operating conditions, and the internal 50-ohm resistors avoid the need for external terminations for impedance matching. The DM7080 uses SCFL I/O levels and allows either single-ended or differential data input and output. An on-chip output buffer provides an excellent eye diagram at a 12.5 GHz clock frequency.

Features

- Ultra wideband: Up to 12.5 Gb/s
- 900 mVpp single ended output dynamic
- Output rise time (20%-80%): 28 ps
- Output fall time (20%-80%): 27 ps
- DC coupled clock input
- DC coupled data input
- Peak-to-peak Jitter < 5 ps
- 50 ohm matched DC-coupled data output
- Differential or single-ended inputs
- Low power consumption:
  800 mW at -5 V (VQH = 0.0 V, VQL = -0.9 V)
- Available in Die Form or 4mm QFN 16L
  0.65mm Pitch plastic package

Device Diagram



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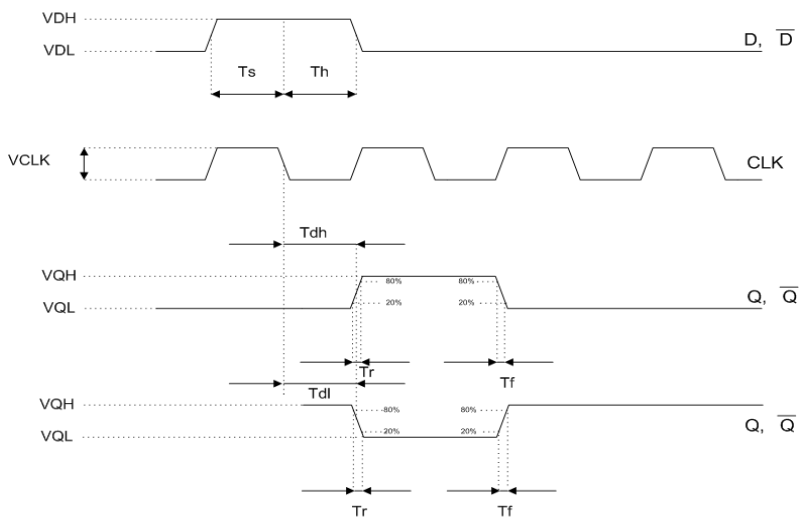
Timing Diagram



Absolute Maximum Ratings

Stresses in excess of those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
Vee	Power supply voltage	-5.5	0	V
VDH	Data/clock input voltage level, high level	-1.2	1.2	V
VDL	Data/clock input voltage level, low level	-1.2	1.2	V
Ta	Operating temperature range – die	-15	125	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Ta	Operating temperature range – die	0		85	°C
Vee	Power supply voltage		-5.0		V
Vindc	Data DC input voltage common mode	-0.4	0	0.1	V
Vinpp	Data input voltage level (single-ended, peak-to-peak)		0.5		V
VCLKdc	Clock input voltage common mode		0		V
VCLK	Clock input voltage (single-ended, peak-to-peak)		0.7		V

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Electrical Characteristics

Symbol	Parameters	Min	Typ	Max	Units
Vee	Power supply voltage	-5.45	-5.0	-4.70	V
VCLK	Input clock voltage amplitude	0.4	0.7	1.0	V
VCLKdc	Input clock voltage common mode	-0.5	0	0.1	V
VDH	Data input voltage level, high level (single ended) (2)	-0.6	0.25	0.6	V
VDL	Data input voltage level, low level (single ended) (2)	-1	-0.25	0.6	V
Vinppd	Data/clock input voltage level differential peak to peak	0.50	1.0	2.0	
Vindc	DC input voltage (with DC-coupled input) (3)	-0.75	0	0.25	V
VQH	Data output voltage amplidude high	-0.05	0	0	V
VQL	Data output voltage amplidude low	-1.1	-0.85	-0.4	V
Tr	Output rise time (20% - 80%)		26		ps
Tf	Output fall time (20% - 80%)		26		ps
Tdl	Output fall delay (CLK vs. Q,Qb) (4)		63		ps
Tdh	Output rise delay (CLK vs. Q,Qb) (4)		65		ps
Ts	Minimum setup time (7)		14		ps
Th	Minimum hold time (7)		14		ps
PM1	Phase margin at 12.5 Gb/s NRZ input (5) (8)	220	240	260	deg
PM2	Phase margin at 10.7 Gb/s NRZ input (5) (8)	230	250	270	deg
FMAx	Clock frequency (6)	0		13	GHz
RMAx	Input data rate (6)	0		13	Gb/s
RLin	Minimum input return loss (up to 13 GHz)		10		dB
RLout	Minimum output return loss (up to 13 GHz)		10		dB
Jpp	Peak to peak jitter at 12.5 Gb/s	3	4.5	6	ps
Jrms	RMS jitter		0.8		ps
Ic	Power supply current		160		mA
Pd	Power dissipation		800		mW

1. Electrical characteristics at ambient temperature.

2. Minimum and maximum values for VDH and VDL have to be set in order to satisfy the following rule: 0.2 V <(VDH -VDL) <1 V

3. In case of single-ended input, the unused one must be tied to Vindc which must be nominally set to the applied input mean value.

4. Output change state on input rising edge.

5. Calculated as follows in the following equation:

$$PM[deg]=\frac{PM(meas)*360[deg]}{BitDuration}$$

where:

$$BitDuration[ps]=\frac{1}{BitRate[Gb/s]}$$

and PM and BitDuration are measured in ps

6. Duty cycle 50%. Asymmetrical duty cycle may reduce maximum frequency.

7. @ 10.7Gb/s

8. for B.E.R. < 10^{-12}

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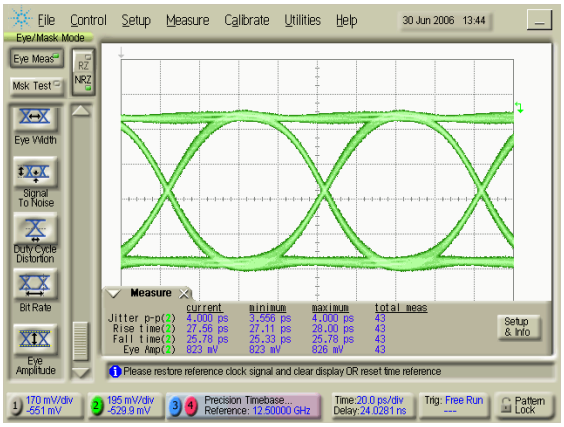
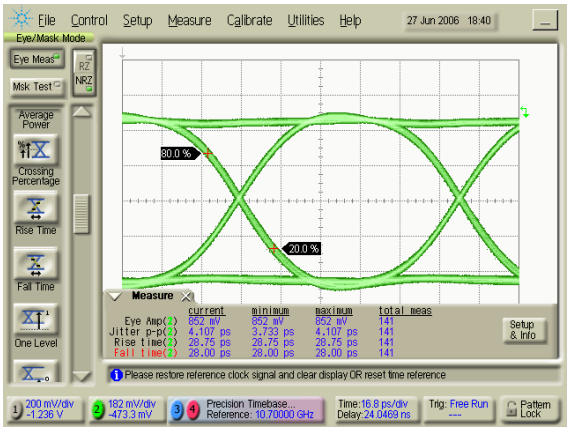
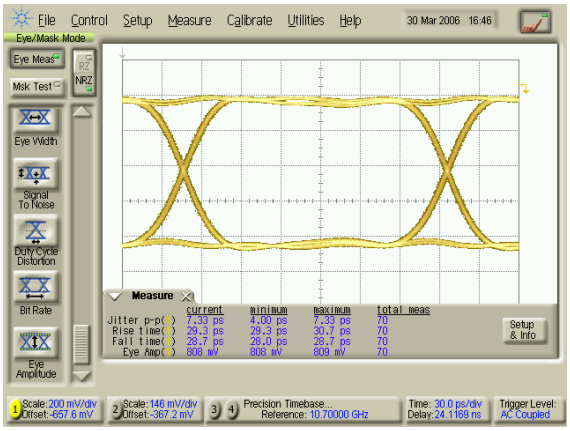
Eye Diagram Performance



Output at 12.5 Gb/s. Power supply = -5 V



Output at 10.7 Gb/s. Power supply = -5 V



Output at 5 Gb/s. Power supply = -5 V

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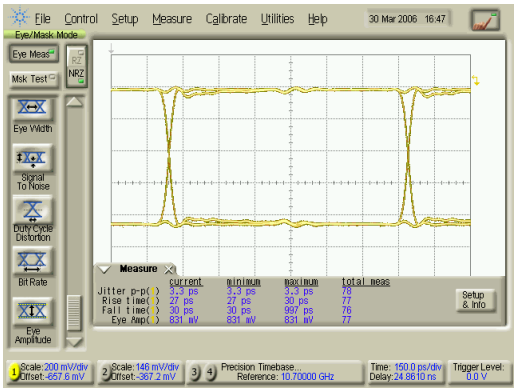
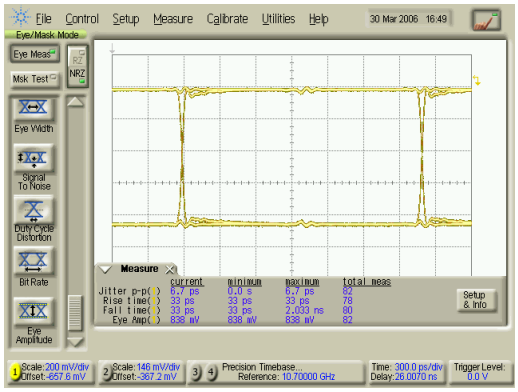
Eye Diagram Performance (cont.)



Output at 1 Gb/s

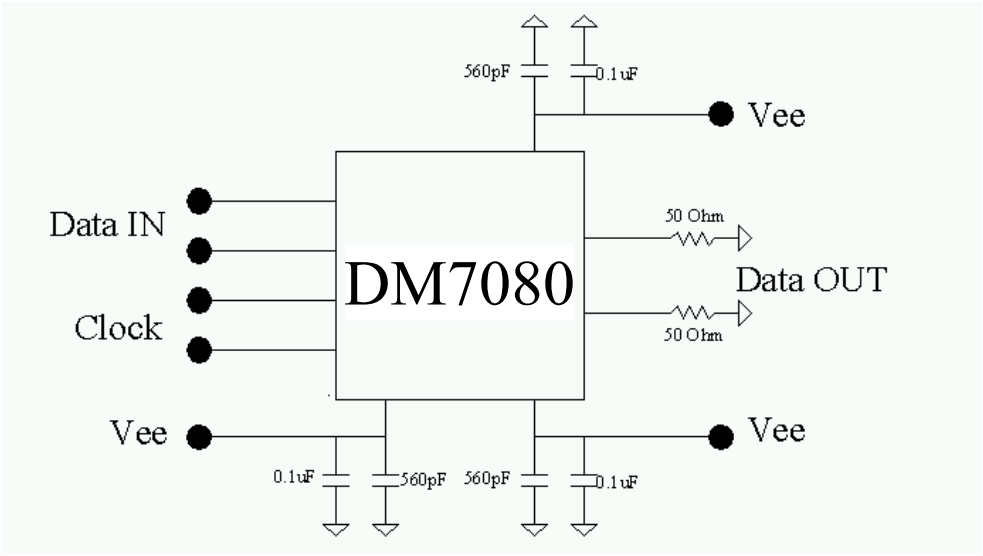


Output at 500 Mb/s

Recommended Operational Setup

Bias Conditions

Connect Ground and Vee
Connect inputs
Apply -5.0 V at Vee
Apply RF signals to the inputs
Tune Vindc for optimal eye diagram in case of single-ended input.



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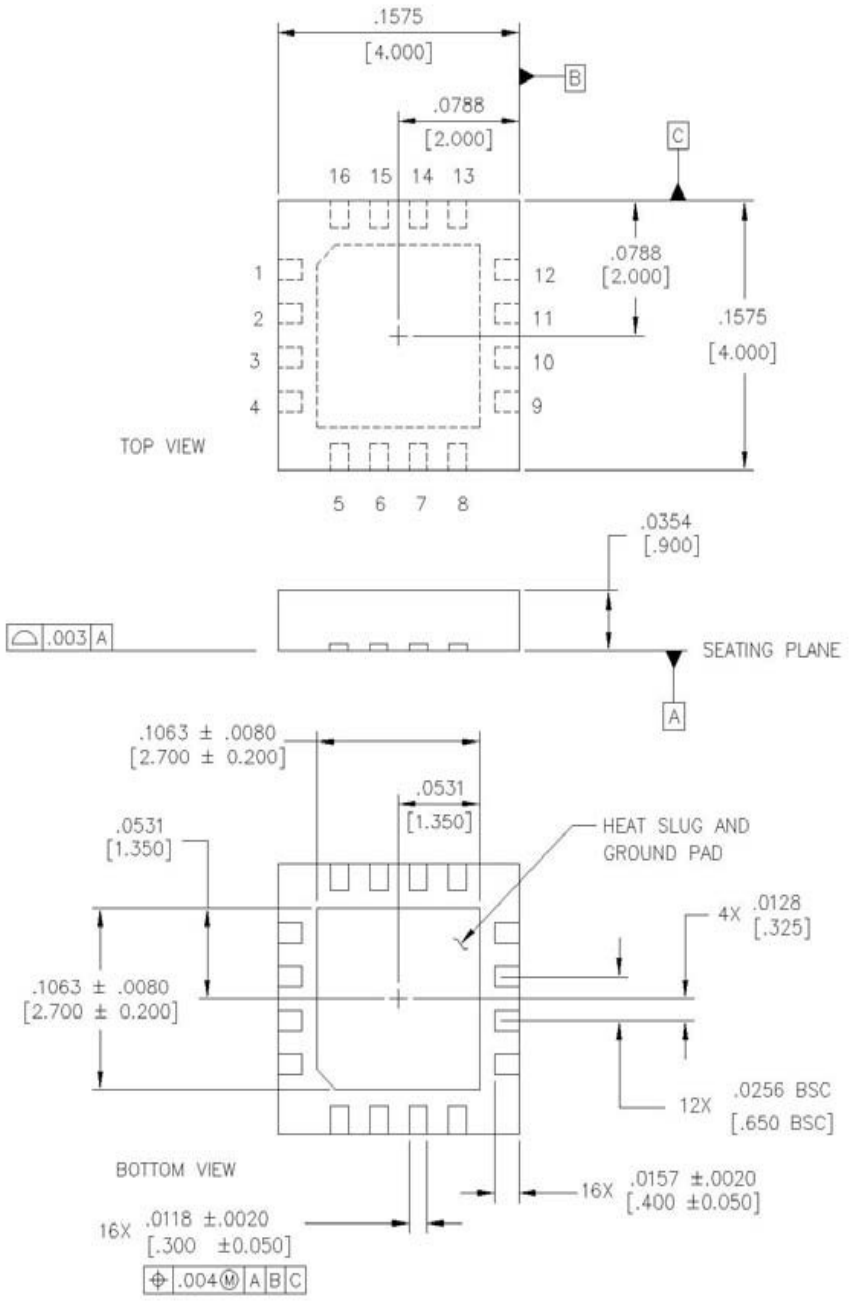
Package Drawing and Pinouts

Dimension: Inches[mm]
Name equivalencies
Din = Data Input
Clck = Clock Input
Q = Data Output
VEE=Power Supply



Pinouts

P1: A	**P9: Vee**
P2: N/C	**P10: Dout**
P3: A/	**P11: N/C**
P4: Vee	**P12: Dout/**
P5: B	**P13: Vee**
P6: N/C	**P14: N/C**
P7: B/	**P15: N/C**
P8: N/C	**P16: N/C**

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for HBT devices. Note that the backside of the chip is gold plated and it is connected to RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding: for Signal input / output connections, use either 3 mils wide and 0.5 mil thick gold ribbon or a pair of 1mil diameter wires with lengths as short as practical allowing for appropriate stress relief (typically 400 +/- 100 um long). For all other connections, a single 1 mil dia wire of appropriate minimum length may be used.

Product Status Definitions

Datasheet Identification	Product Status	Definition
Advanced Information	Formative or or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not in Production	This datasheet contains specifications on a product that has been discontinued by DIGIMIMIC. The datasheet is printed for reference information only.

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