

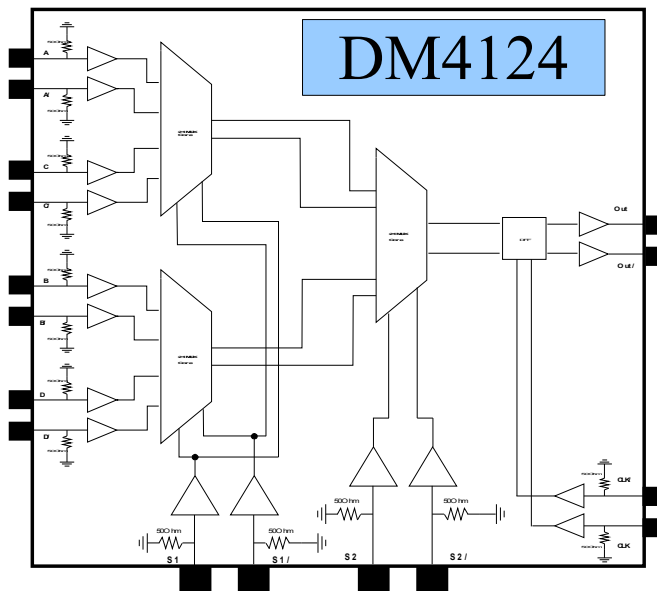
### Description

The DM4124 is an ultra-high-speed, 4-to-1 multiplexer that provides high performance and is easy to use for implementing static or dynamic four-to-one multiplexing of LVSCFL-like signals with an **aggregate data rate up to 12.5 Gb/s**. Its wide operating frequency range makes it useful in many situations for the interfacing of low-speed devices to high-speed devices. **Both static switch and dynamic 4:1 multiplexer operating modes are supported.** The DM4124 is fabricated using HBT InP technology and it has been designed using an ECL topology to ensure high-speed operation. DM4124 has 50 ohm resistor terminations on data inputs (A, B,C,D - DC coupled) and a wide spread of allowable differential voltage levels [0.4V to 1.6V] so to guarantee full compatibility with 3.3VLVSCFL devices. All control signal (S1,S2,Clk) are DC or AC coupled, LVSCFL (ViH=3.3V ViL=2.85V), with internal 50 ohm resistors to Vcc. The output of the DM4124 is DC coupled with 450-mVpp single-ended amplitude LVSCFL (VoH=3.3V VoL=2.75V). The four to one core mux is followed by an internal DFF so to improve jitter performances. The high-performance output buffer provides an excellent eye diagram up to 12.5 Gb/s NRZ output. The DM4124 uses one single power supply (3.3V) while power consumption is lower than 0.4W

### Features

- **Data Input (A,B,C,D) LVSCFL:**
  - Common Mode Range [0V,0.4V]
  - Differential PP range [0.4V,1.6V]
  - 50 ohm to GND internal resistor
  - DC Coupling
- **Control Inputs (S1,S2,Clk) LVSCFL levels:**
  - sensitivity >200 mV
  - VH Typical 3.3V
  - VL Typical 2.85V
  - 50 ohm to GND internal resistors
  - AC or DC coupling allowed
- **Output**
  - **Range: DC to 12.5 Gb/s**
  - 450 mVpp typical single-ended output
  - Output rise time (20% - 80%): <24 ps
  - Output fall time (20% - 80%): <24 ps
  - **Power consumption: lower than 350 mW**
  - Power Supply Vee=-3.3V
  - Available in Die or plastic QFN 5mmx5mm 32L

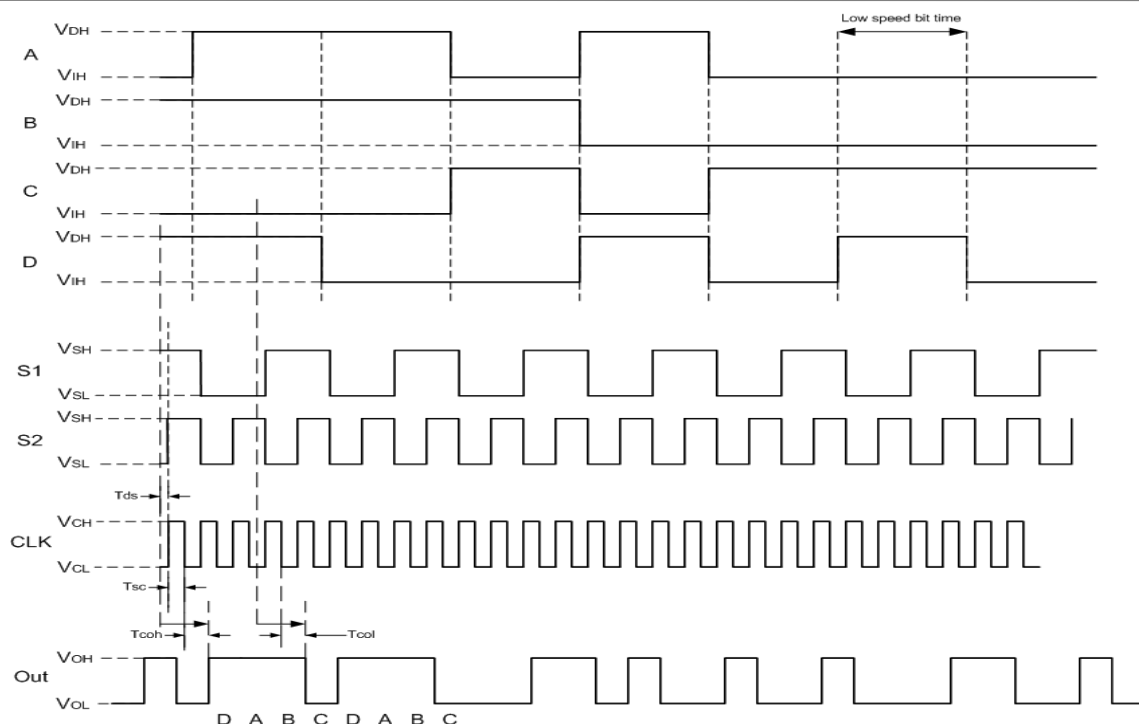
### Device Diagram



### Disclaimer

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### Timing Diagram



### Absolute Maximum Ratings

Stresses in excess of those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
V <sub>ee</sub>	Power supply voltage	-3.3	0	V
V <sub>DH</sub>	Data/selecter input voltage level, high level	-1	1	V
V <sub>DL</sub>	Data/selecter input voltage level, low level	-1	1	V
T <sub>a</sub>	Operating temperature range	-5	85	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

### Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
T <sub>a</sub>	Operating temperature range – die	0		85	°C
V <sub>ee</sub>	Power supply voltage		-3.3		V
V <sub>DH</sub>	Data/clock input voltage level, high level (single ended)	-0.1	0.25		V
V <sub>DL</sub>	Data/clock input voltage level, low level (single ended)	-0.5	-0.25		V
V <sub>indc</sub>	DC input voltage (with DC-coupled input)	-0.3	0		V
V <sub>ipp</sub>	Data/clock input voltage level (single Ended peak to peak)		0.2		V



# DM4124

## 4:1 Mux With Output Sampling DFF (Advanced Information)

### Electrical Characteristics

1. Electrical characteristics at ambient temperature.

2. In case of single-ended inputs the unused ones must be tied to Vindc which must be set close to the mean value of the used one. For AC single-ended inputs having 0 V mean value, the unused inputs may be left floating.

3. Output referred to selector rising edge.

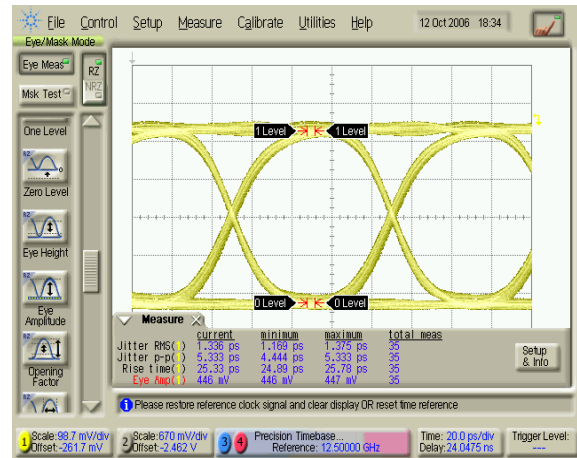
4. Duty cycle 50%. Asymmetrical duty cycle may reduce maximum operating data rate.

Symbol	Parameters	Min	Typ	Max	Units
Vee	Power supply voltage	-3.45	-3.3	-3.15	V
VDH	Data/clock/selector input voltage level, high level (single ended)	-0.25	0	0.25	V
VDL	Data/clock/selector input voltage level, low level (single ended)	-0.75	-0.5	-0.25	V
Vindiff <sub>pp</sub>	Data/clock/selector input voltage level differential peak to peak	0.40	0.80	1.0	V
Vindc	DC input voltage (with DC-coupled input) <sup>(2)</sup>	-0.5	-0.25	0.0	v
VQH	Data output voltage amplitude high	-0.05	0	0	v
VQL	Data output voltage amplitude low	-0.40	-0.45	-0.50	v
Tr	Output rise time (20% - 80%)		22		ps
Tf	Output fall time (20% - 80%)		20		ps
FMAx	Clock frequency Input	0	12.6	13	GHz
RMAx	Input data rate <sup>(4)</sup>	0	3.15	12.6	Gb/s
RLin	Minimum Input return loss (up to 15 GHz)				dB
RLout	Minimum output return loss (up to 15 GHz)				dB
Jpp	Peak to peak jitter		5.3		ps
Jrms	RMS jitter		1.3		ps
Ic	Power supply current		110		mA
Pd	Power dissipation		0.35		W

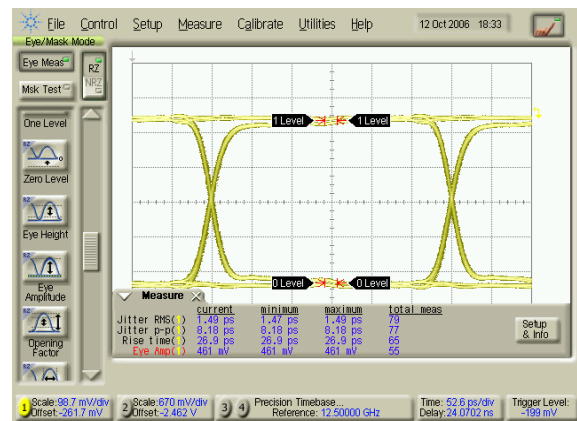
S1	S2	OUT
L	L	A
L	H	B
H	L	C
H	H	D

### Eye Diagram Performance

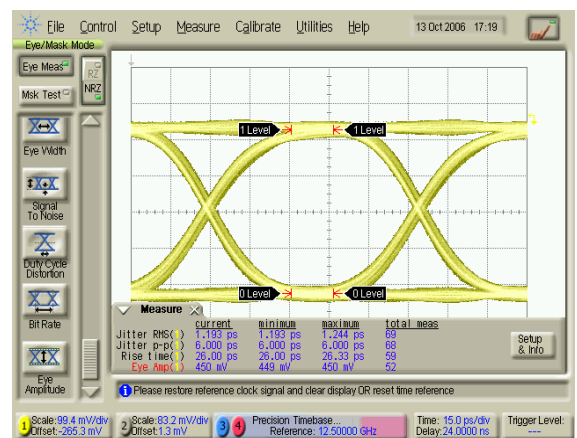
EVB Measurement  
Static Switch  
Vee: -3.3 V  
Output data rate: 12.5 Gb/s  
Data input: 300 mVpp SE



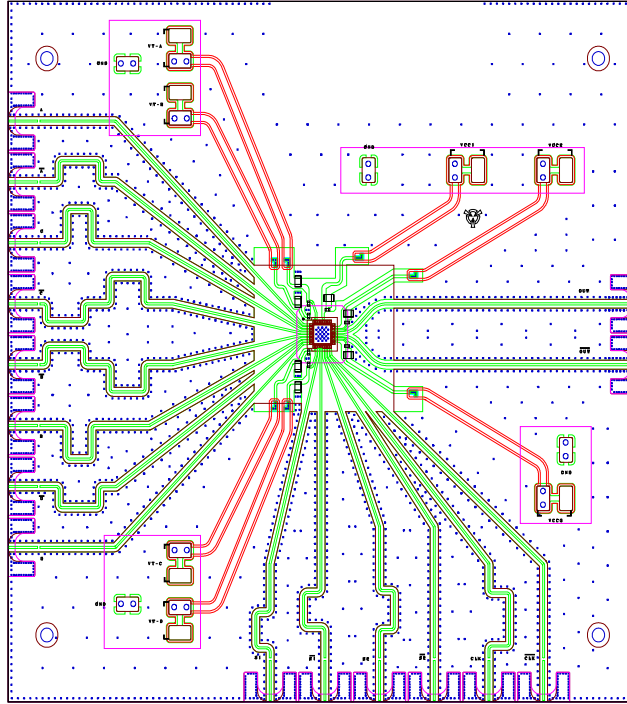
EVB Measurement  
Static Switch  
Vee: -3.3 V  
Output data rate: 2.5 Gb/s  
Data input: 300 mVpp SE



EVB Measurement  
Dynamix 4:1 Mux  
Vee: -3.3 V  
Output data rate: 12.5 Gb/s  
Data input: 300 mVpp SE



**EVB  
Evaluation Board**



**Power Up  
Sequence  
A**

**Connect Cables  
Apply -3.3V at Vee, Iee=110mA approx.  
Apply signals**

**Typical Values**

	Vee V	Iee mA	
Bias	-3.3	110	

### Application Information

**CAUTION: THIS IS AN ESD SENSITIVE DEVICE**

Chip carrier material should be selected to have InP compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for HBT devices. Note that the backside of the chip is gold plated and it is connected to RF and DC Ground.

These InP devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding: for Signal input / output connections, use either 3 mils wide and 0.5 mil thick gold ribbon or a pair of 1mil diameter wires with lengths as short as practical allowing for appropriate stress relief (typically 400 +/- 100 um long). For all other connections, a single 1 mil dia wire of appropriate minimum length may be used.

### Product Status Definitions

Datasheet Identification	Product Status	Definition
Advanced Information	Formative or or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not in Production	This datasheet contains specifications on a product that has been discontinued by DIGIMIMIC. The datasheet is printed for reference information only.