DM4122A
2:1 Combinatorial Mux
AND/OR Programmable Logic Gate
(Advanced Information)

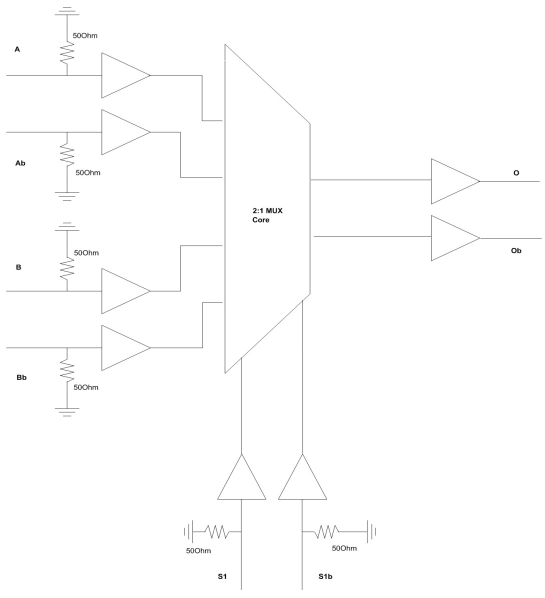
Description

The DM4122AD is an ultra-high-speed, 2-to-1 multiplexer that provides high performance and is easy to use for implementing static or dynamic two-to-one multiplexing. Its wide operating frequency range makes it useful in many situations for the interfacing of low-speed devices to high-speed devices. Both static full-rate switch and dynamic 2:1 multiplexer operating modes are supported. The DM4122AD is fabricated using 1-µm HBT GaAs technology and it has been designed using an ECL topology to ensure high-speed operation. Both data inputs (A, B) and control signal (S1) are DC coupled with internal 50-ohm resistors to avoid the need for external impedance matching terminations. The DM4122AD uses SCFL input levels (VIH: 0.0 V, VIL: -0.9 V), and is designed to allow either single-ended or differential data input. AC coupling through an external capacitor is also possible. The output of the DM4122AD is DC coupled with 900-mVpp single- ended amplitude. An on-chip, high-performance output buffer provides an excellent eye diagram up to 12.5 Gb/s RZ output. The DM4122AD combinatorial multiplexer may also be used as an OR- AND gate and the high quality of the output buffer allows it to be used as a 12.5-Gb/s NRZ-to-RZ converter.

Features

- Output data rate range: DC to 12.5 Gb/s
- 900 mVpp typical single-ended output
- Single-ended input sensitivity: >300 mV
- 1.2 ps jitter RMS
- Output rise time (20% - 80%): <27 ps
- Output fall time (20% - 80%): <24 ps
- Full SCFL input level compatibility
- 50 ohm matched AC/DC coupled input and outputs, clock input, and selector input
- Differential or single-ended I/O
- Up to 12.5 Gb/s NRS-to-RZ converter, AND/OR logic implementation, static switch, or multiplexer
- Power consumption: 0.715 W

Device Diagram



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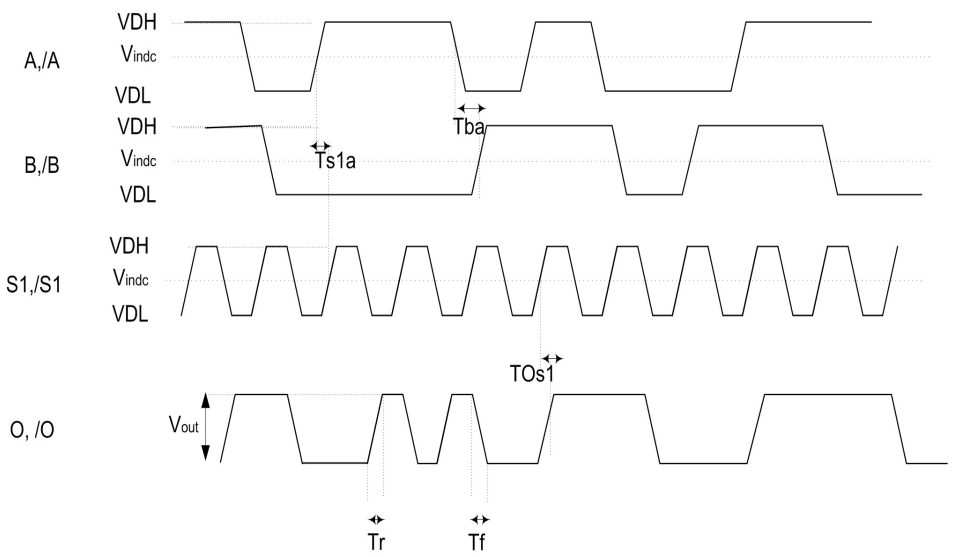
Timing Diagram



Absolute Maximum Ratings

Stresses in excess of those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
Vee	Power supply voltage	-5.5	0	V
VDH	Data/clock input voltage level, high level	-1.2	1.2	V
VDL	Data/clock input voltage level, low level	-1.2	1.2	V
Ta	Operating temperature range – die	-15	125	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
Ta	Operating temperature range – die	0		85	°C
Vee	Power supply voltage		-5.2		V
VDH	Data/clock input voltage level, high level (single ended)	-0.1	0.25		V
VDL	Data/clock input voltage level, low level (single ended)	-0.6	-0.25		V
Vindc	DC input voltage (with DC-coupled input)	-0.3	0		V
Vipp	Data/clock input voltage level (single Ended peak to peak)		0.5		V

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Electrical Characteristics

Symbol	Parameters	Min	Typ	Max	Units
Vee	Power supply voltage	-5.45	-5.2	-4.85	V
VDH	Data/clock/selector input voltage level, high level (single ended)	-0.5	0.25	0.5	V
VDL	Data/clock/selector input voltage level, low level (single ended)	-1	-0.25	0	V
Vindiffpp	Data/clock/selector input voltage level differential peak to peak	0.40	1.0	1.8	V
Vindc	DC input voltage (with DC-coupled input)[2]	-0.75	0	0.25	V
VQH	Data output voltage amplitude high	-0.05	0	0	V
VQL	Data output voltage amplitude low	-0.95	-0.9	-0.85	V
Tr	Output rise time (20% - 80%)		27		ps
Tf	Output fall time (20% - 80%)		24		ps
Tos1	S1 to output delay [3]				ps
Ts1a	Input to S1 time window				ps
Tba	Data Input time shift				ps
FMAx	Clock frequency Input	0	12.6	13	GHz
RMAx	Input data rate [4]	0	6.3	6.5	Gb/s
RLin	Minimum Input return loss (up to 15 GHz)				dB
RLout	Minimum output return loss (up to 15 GHz)				dB
Jpp	Peak to peak jitter		10		ps
Jrms	RMS jitter		1.5		ps
Ic	Power supply current		138		mA
Pd	Power dissipation		0.715		W

1. Electrical characteristics at ambient temperature.

2. In case of single-ended inputs the unused ones must be tied to Vindc which must be set close to the mean value of the used one. For AC single-ended inputs having 0 V mean value, the unused inputs may be left floating.

3. Output referred to selector rising edge.

4. Duty cycle 50%. Asymmetrical duty cycle may reduce maximum operating data rate.

Truth table	
S1	Out
H	A
L	B

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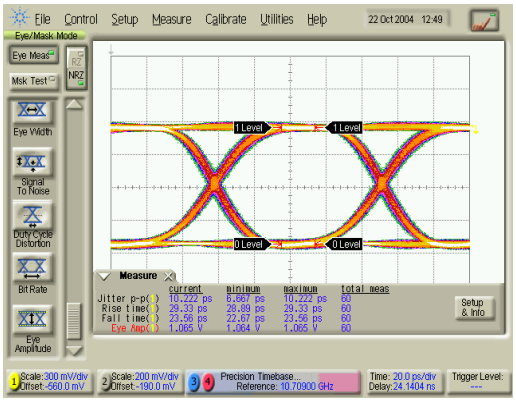
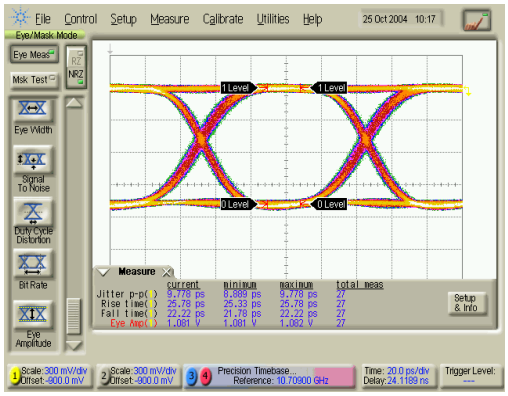
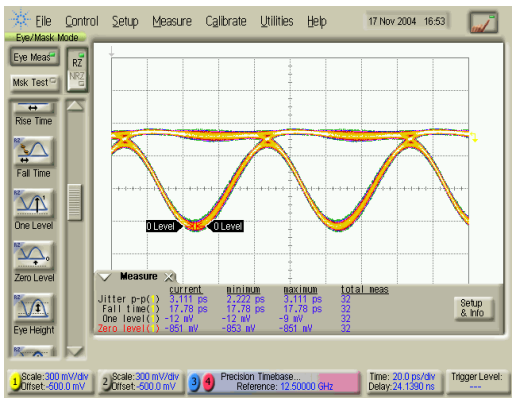
Eye Diagram Performance



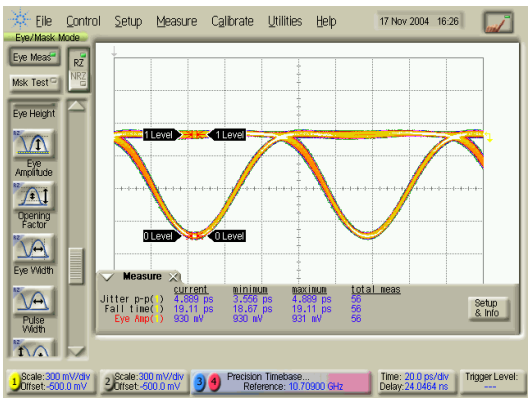
Test board measurement
Vee: -5.2 V + 5% = -4.95 V
Output data rate: 10.7 Gb/s
Data input: 900 mVpp SE
S1 input 900 mVpp SE



Test board measurement static switch
Vee: -5.2 V + 5% = -4.95 V
Output data rate: 10.7 Gb/s
Data input: 900 mVpp SE



Test board measurement RZ converter
Vee: -5.2 V+ 5% = -4.95 V
NRZ input rate: 12.5 Gb/s
Data input: 900mVpp SE
Clock Input: 900 mVpp SE



Test board measurement RZ converter
Vee: -5.2 V + 5% = -4.95 V
NRZ input rate: 10.7 GHz
Data input: 900 mVpp SE
Clock input: 900 mVpp SE

Disclaimer

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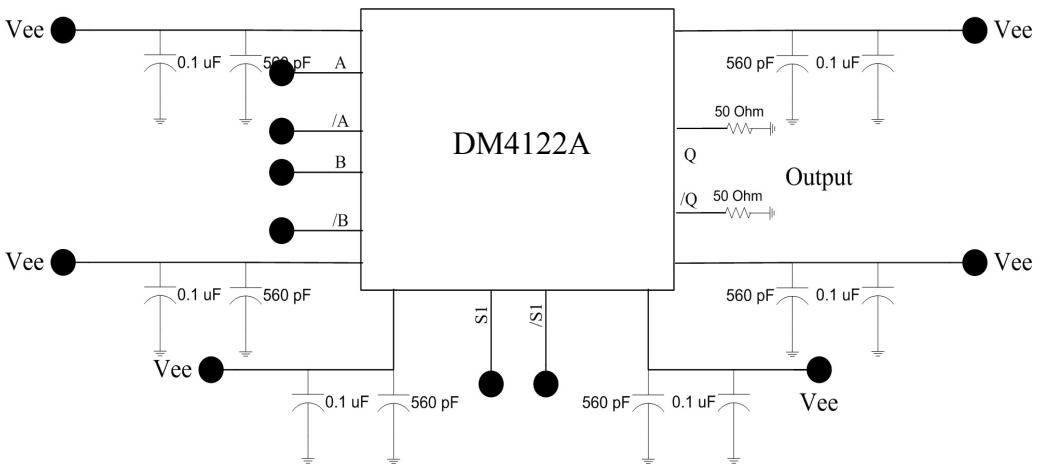
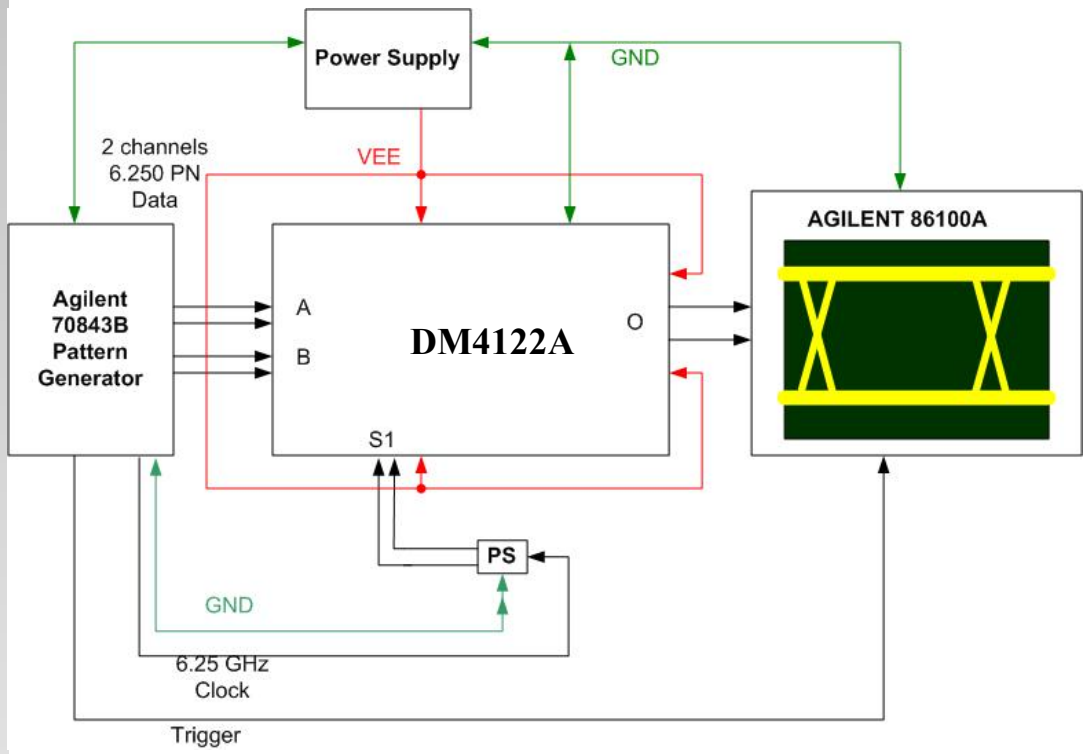
Recommended Operational Setup

Bias Conditions

1. Connect inputs to a fixed DC value
2. Apply -5.2 V at Vee
3. Apply RF signals to the inputs
4. Tune Vindc for optimal eye diagram in case of single-ended inputs.



Recommended Test Setup



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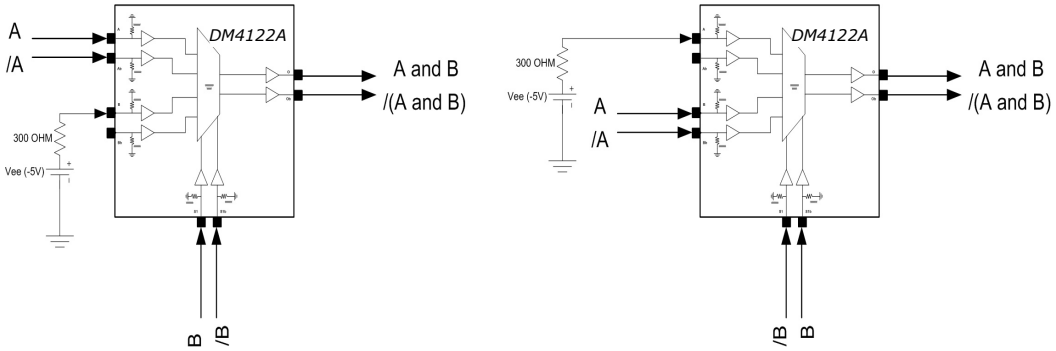
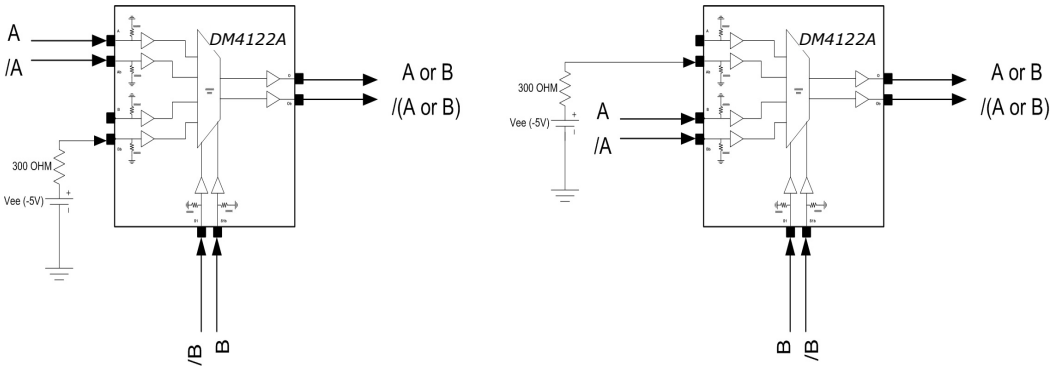
Logic AND Gate Configuration

The DM4122AD may be used in place of a logic AND gate by simply feeding one data input and the selector input with the two data streams and setting the unused one to logical "0" (for example using a 300-ohm pull-down to Vee).



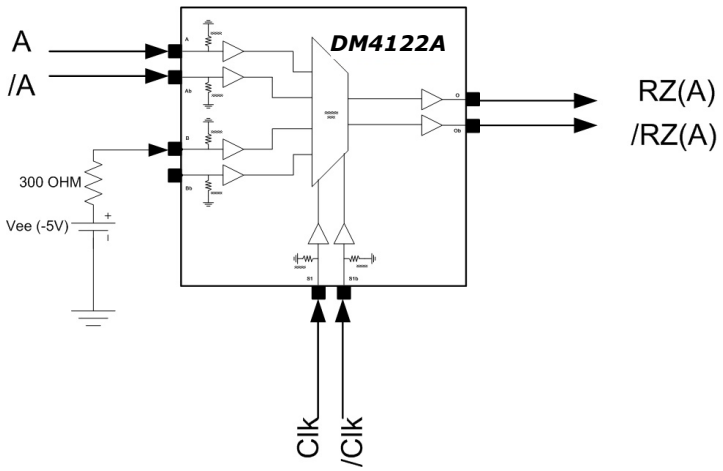
Logic OR Gate Configuration

The unused input must be fixed at logic "1".



NRZ-To-RZ Converter

The NRZ-to-RZ converter is demanding from a bandwidth point of view. It is basically the AND between input PN data and a clock.



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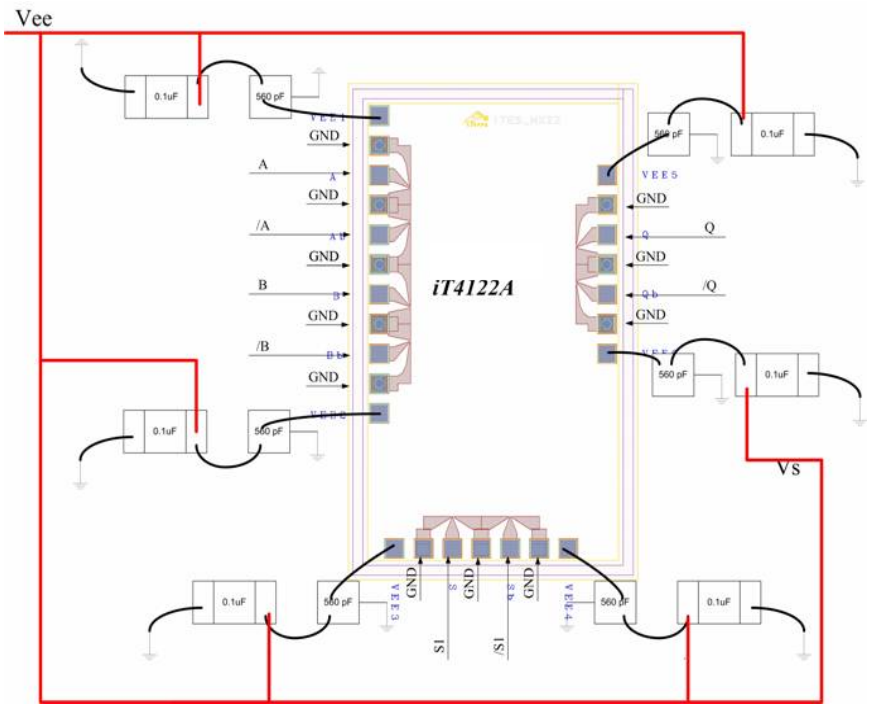
Recommended Chip Mounting



Pad Positions And Chip Dimensions

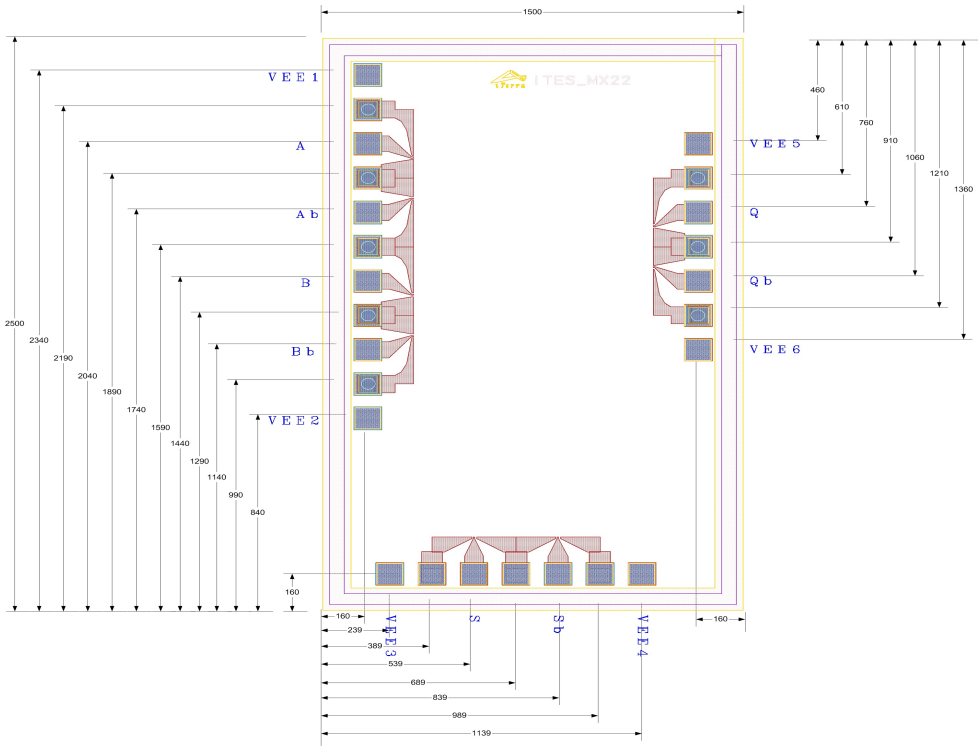
Chip size:
1500 µm ±10 µm x 2500 µm ±10 µm edge to edge

Chip thickness:
104 µm ±3 µm

Pad size:
100 µm x 100 µm

RF pad pitch:
150 µm

Unlabeled pads are ground and may be left floating



Specifications are based on most current or latest revision.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have InP compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for HBT devices. Note that the backside of the chip is gold plated and it is connected to RF and DC Ground.

These InP devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding: for Signal input / output connections, use either 3 mils wide and 0.5 mil thick gold ribbon or a pair of 1mil diameter wires with lengths as short as practical allowing for appropriate stress relief (typically 400 +/- 100 um long). For all other connections, a single 1 mil dia wire of appropriate minimum length may be used.

Product Status Definitions

Datasheet Identification	Product Status	Definition
Advanced Information	Formative or or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not in Production	This datasheet contains specifications on a product that has been discontinued by DIGIMIMIC. The datasheet is printed for reference information only.

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