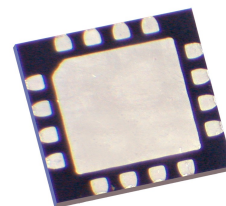


### Description

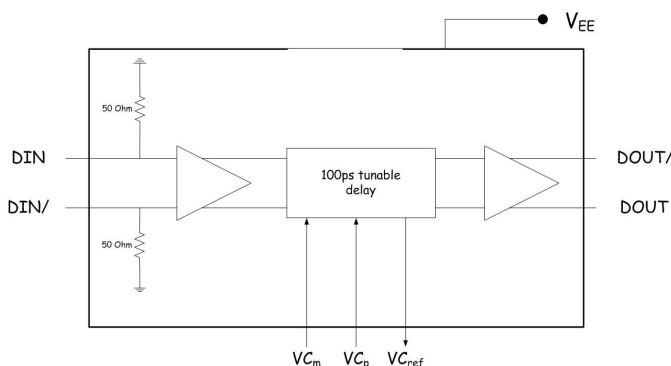
The DM4031 is an ultra-wideband phase delay fabricated using 1-um HBT GaAs technology and is based on ECL topology to guarantee high-speed operation. The high output voltage, excellent rise and fall time, and the high eye diagram quality at data rates to 12.5 Gb/s makes the DM4031 suitable for timing adjustment in data and clock distribution at very high speed. Complex digital applications benefit from the DM4031, including clock data recovery, edge detectors, NRZ-to-RZ converters, MUX/DEMUX, and data restoration. The device features a single delay element that provides up to 100-ps delay. Delay control can be either differential (using both VCp and VCm) or single-ended (VCm is the active control pad while VCp is shorted to VCref). The control voltage range for the delay input is from -2.2 V to -3.0 V whether the control is single-ended or differential. The device can delay NRZ streams with data rates to 12.5 Gb/s or a clock signal up to 10.7 GHz. Both inputs and outputs are DC-coupled. At the input side, internal 50-ohm resistors avoid the need for external impedance matching terminations. The DM4031 uses SCFL I/O levels and is designed so to allow for either single ended or differential data input.

### Features

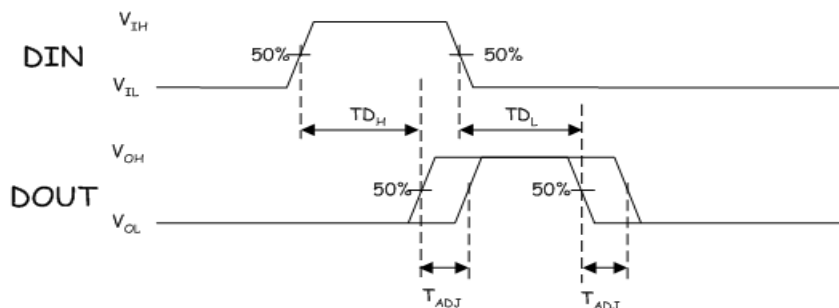
- ❖ Ultra wideband: Up to 12.5 Gb/s NRZ
- ❖ Delay adjustment to 100 ps
- ❖ 900 mVpp single-ended output
- ❖ Jitter RMS: <1.5 ps
- ❖ Output rise time (20% – 80 %): <25 ps
- ❖ Output fall time (20% – 80 %): <23 ps
- ❖ 50-ohm matched DC-coupled inputs and outputs
- ❖ Differential or single ended I/O
- ❖ Power consumption: 1.65 W



### Device Diagram



### Timing Diagram



### Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
VEE	Power supply voltage	-5.5	0	V
VIH	Input voltage level, high level	-1.5	1.5	V
VIL	Input voltage level, low level	-1.5	1.5	V
VC	Delay control voltage	-5.0	0	V
TA	Operating temperature range – die	-15	125	°C
TSTG	Storage temperature	-65	150	°C

### Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
T <sub>A</sub>	Operating temperature range – die	0		85	°C
V <sub>EE</sub>	Power supply voltage		-5		V
VC	Delay control voltage	-3.0	-2.6	-2.2	V
V <sub>IH</sub>	Input voltage level, high level (single ended)		0.0		V
V <sub>IL</sub>	Input voltage level, low level (single ended)		-0.9 0.4		V
V <sub>INDC</sub>	DC input voltage (with DC-coupled input)		5		V

### Electrical Characteristics

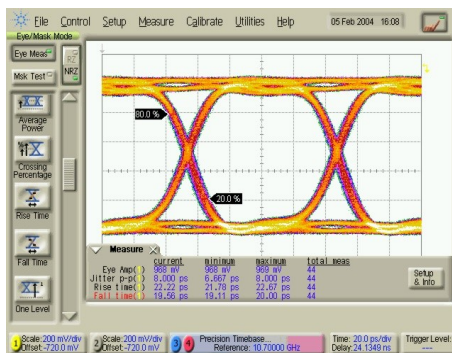
1. Electrical characteristics at ambient temperature.
2. In case of single-ended input, the unused pad must be tied to V<sub>INDC</sub>.
3. In case of single-ended output, the unused pad must be terminated with 50 ohms to ground.
4. Refer to timing diagram.
5. On a 10.7 Gb/s PRBS pattern.

Symbol	Parameters	Min.	Typ.	Max.	Units
VEE	Power supply voltage	-4.5	-5.00	-5.25	V
VIH	Input voltage level, high level (single ended)		0.0		V
VIL	Input voltage level, low level (single ended)		-0.9		V
VINDC	DC input voltage (with DC-coupled input) (2)		-0.45		V
VOUT	Data output voltage amplitude (3)	0.8	0.9	1.0	V
TR	Output rise time (20% – 80%)		25		ps
TF	Output fall time (20% – 80%)		23		ps
TDH	Output delay low-high transition (4)		300		ps
TDL	Output delay high-low transition (4)		300		ps

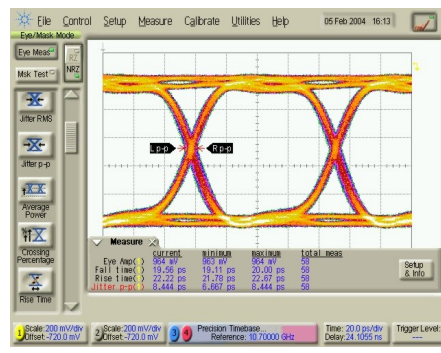
### Electrical Characteristics (cont.)

Symbol	Parameters	Min.	Typ.	Max.	Units
$T_{ADJ}$	Output phase delay adjustment <sup>(4)</sup>		100		ps
$S_{11}$	Input return loss (up to 15 GHz)		24		dB
$S_{22}$	Output return loss (up to 15 GHz)		3.4		dB
$F_{MAX}$	Maximum clock frequency		10.7		GHz
$J_{p-p}$	Peak-to-peak jitter <sup>(5)</sup>		9		ps
$J_{rms}$	RMS jitter <sup>(5)</sup>		1.5		ps
$I_{EE}$	Power supply current		330		mA
$P_D$	Power dissipation		1.65		W

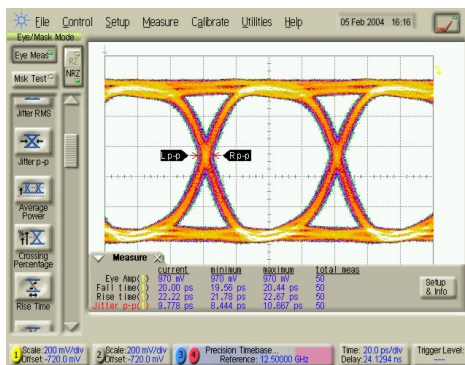
### Eye Diagram Performance



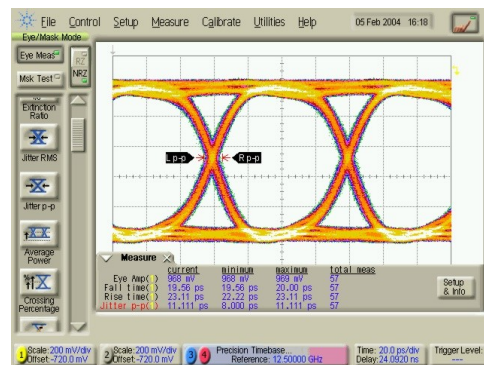
Evaluation board measurement  
Vee: -5.0 V  
Input data rate: 10.7 Gb/s  
Single-ended data input: +/-450 mVpp  
Control voltage: VCP = VCref, VCM = -2.2 V



Evaluation board measurement  
Vee: -5.0 V  
Input data rate: 10.7 Gb/s  
Single-ended data input: +/-450 mVpp  
Control voltage: VCP = VCref, VCM = -3.0 V

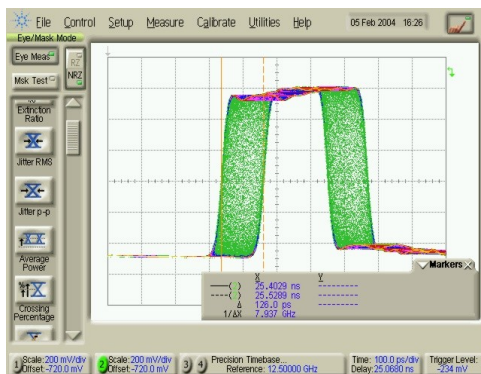


Evaluation board measurement  
Vee: -5.0 V  
Input data rate: 12.5 Gb/s  
Single-ended data input: +/-450 mVpp  
Control voltage: VCP = VCref, VCM = -2.2 V



Evaluation board measurement  
Vee: -5.0 V  
Input data rate: 12.5 Gb/s  
Single-ended data input: +/-450 mVpp  
Control voltage: VCP = VCref, VCM = -3.0 V

### Eye Diagram Performance (cont.)



Evaluation board measurement

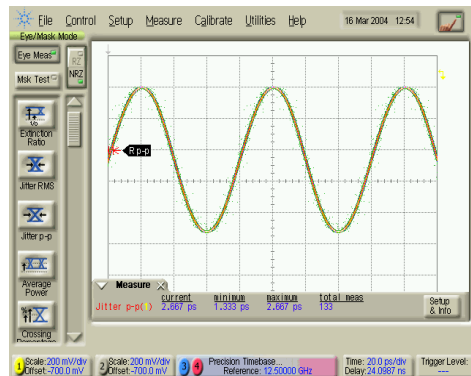
Vee: -5.0 V

Input data rate: 12.5 Gb/s

Single-ended data input: +/-450 mVpp

Control voltage:  $V_{Cp} = V_{Cref}$ ,

$V_{Cm} = -2.2$  to  $-3.0$  V (accumulating)



Evaluation board measurement

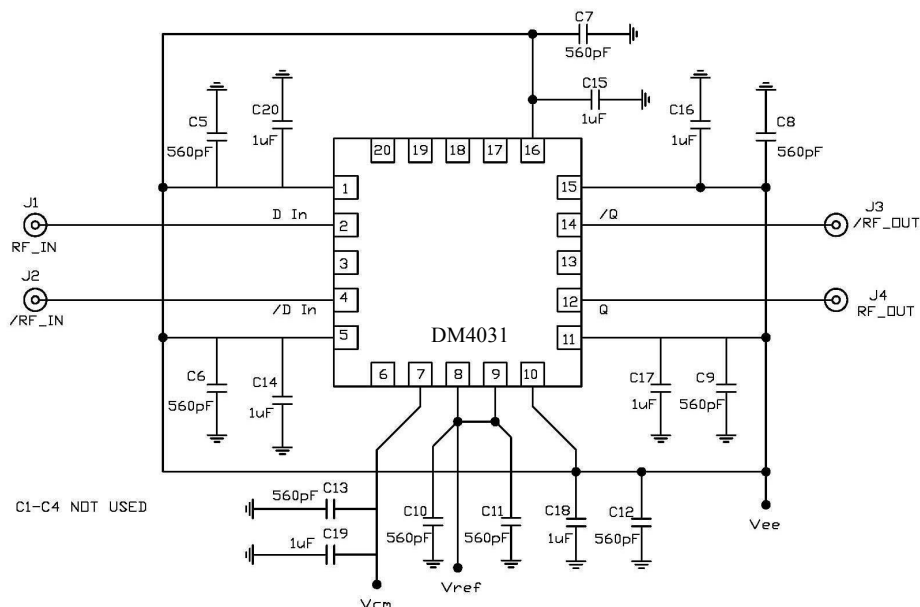
Vee: -5.0 V

Input CLK frequency: 12.5 GHz

Single-ended CLK input: +/-450 mVpp

Control voltage:  $V_{Cp} = V_{Cref}$ ,  $V_{Cm} = -2.2$  V

### Recommended Operational Setup



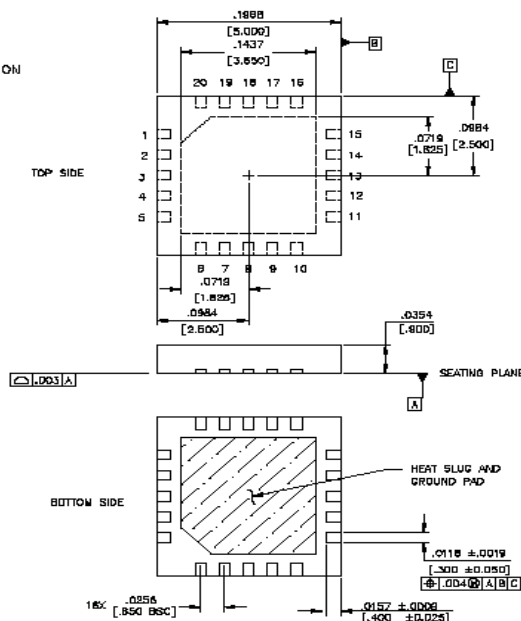
### Package Drawing and Pinouts

#### NOTES

1. DIMENSIONS: INCHES [mm]
2. EXCEPT WHERE NOTED, TOLERANCE ON DIMENSIONS ARE:  $\pm 0.0039$  [0.100]

#### Pinouts:

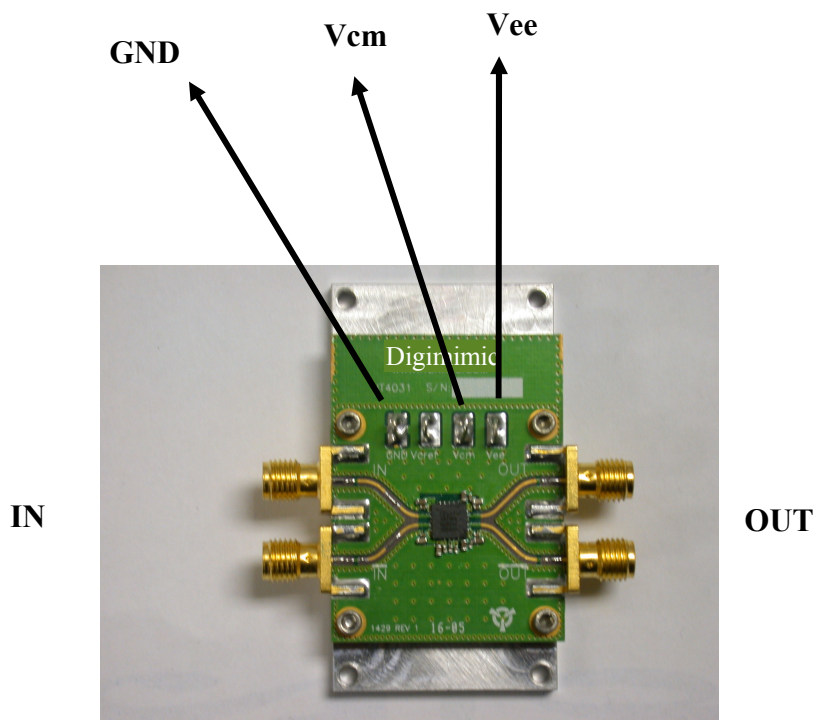
P1: Vee P11: Vee  
 P2: Din P12: Dout  
 P3: N/C P13: N/C  
 P4: Din/ P14: Dout/  
 P5: Vee P15: Vee  
 P6: N/C P16: Vee  
 P7: VCm P17: N/C  
 P8: VCp P18: N/C  
 P9: Vcref P19: N/C  
 P10: Vee P20: N/C



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### EVB Evaluation Board



### Power Up Sequence

Apply  $-5V$  at  $V_{ee}$ ,  $I_{ee}=330mA$  approx.  
Apply  $-2.2V$  at  $V_{cm}$  (control range from  $-2.2$  to  $-3.0V$ )

### Typical Values

	$V_{ee}$ V	$I_{ee}$ mA	$V_{cm}$ V
Bias	-5	330	-2.2 : -3.0

### Application Information

#### CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for HBT devices. Note that the backside of the chip is gold plated and it is connected to RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding: for Signal input / output connections, use either 3 mils wide and 0.5 mil thick gold ribbon or a pair of 1mil diameter wires with lengths as short as practical allowing for appropriate stress relief (typically 400 +/- 100 um long). For all other connections, a single 1 mil dia wire of appropriate minimum length may be used.

### Product Status Definitions

Datasheet Identification	Product Status	Definition
Advanced Information	Formative or or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not in Production	This datasheet contains specifications on a product that has been discontinued by DIGIMIMIC. The datasheet is printed for reference information only.