

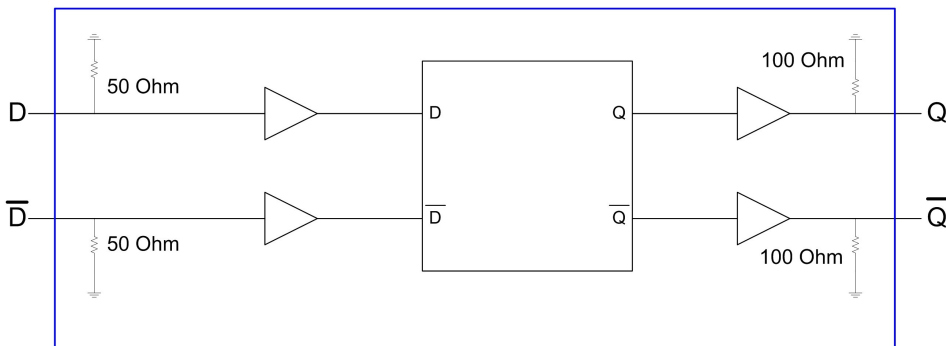
Description

The DM4021 is a high-speed T-type flip-flop fabricated using 1 μ m HBT GaAs technology. The T flip-flop consists of a master-slave latch, closed-in feedback, and is designed using an ECL topology in order to guarantee high-speed operation. The data input may be either AC or DC coupled, the output is DC coupled. At the input side the internal 50-ohm resistors avoid the need for external terminations for impedance matching. The DM4021 uses SCFL I/O levels and is designed to allow for either single-ended or differential data input/output. An on-chip, output buffer produces an excellent eye diagram up to an output rate of 12.5 Gb/s rate (20 Gb/s NRZ or 12.5 Gb/s RZ input data rate) or 14 GHz input clock. The high output voltage, excellent rise and fall times, and the high-quality eye diagram at all clock frequencies makes the DM4021 suitable for very-high-speed, complex digital applications such as differential encoding, clock dividers, and edge detectors.

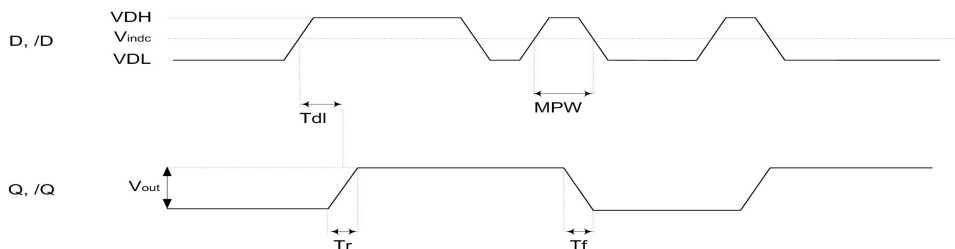
Features

- Data rate range: 20 NRZ (12.5 RZ) Gb/s
- Maximum clock frequency as clock divider: 14 GHz
- 900 mVpp typical single-ended output
- Input sensitivity: Single ended input >250 mV
- Jitter transfer RMS: <1 ps
- Output rise time (20% - 80%): <27 ps
- Output fall time (20% - 80%): <24 ps
- DC or AC coupled data input
- 50-ohm matched DC-coupled data output
- Differential or single-ended inputs and outputs
- Full SCFL I/O level compatibility
- Low power consumption: 0.71 W

Device Diagram



Timing Diagram





DM4021

20 Gb/s (12.5 Gb/s RZ) GaAs MMIC

T-Type Flip-Flop

(Preliminary Information)

Absolute Maximum Ratings

Stresses in excess of those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max	Units
Vee	Power supply voltage	-5.5	0	V
VDH	Data/clock input voltage level, high level	-1.2	1.2	V
VDL	Data/clock input voltage level, low level	-1.2	1.2	V
Ta	Operating temperature range – die	-15	125	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operational Conditions

Symbol	Parameters/conditions	Min.	Typ	Max	Units
Ta	Operating temperature range – die	0		85	°C
Vee	Power supply voltage		-5.2		V
VDH	Data/clock input voltage level, high level (single ended)	-0.1	0.25		V
VDL	Data/clock input voltage level, low level (single ended)	-0.6	-0.25		V
Vindc	DC input voltage (with DC-coupled input)	-0.3	0		V
Vipp	Data/clock input voltage level (single-Ended peak to peak)		0.5		V

Electrical Characteristics

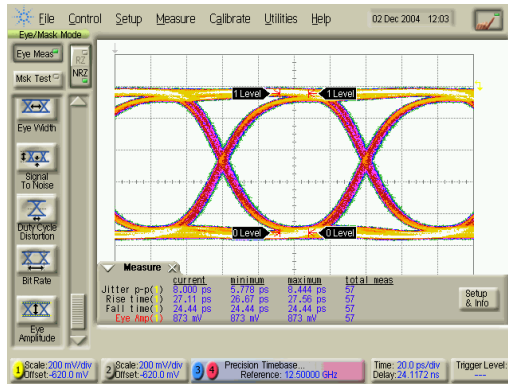
Symbol	Parameters	Min	Typ	Max	Units
Vee	Power supply voltage	-5.45	-5.2	-4.85	V
VDH	Data/clock input voltage level, high level (single ended)	-0.5	0.25	0.5	V
VDL	Data/clock input voltage level, low level (single ended)	-1	-0.25	0	V
Vindiffpp	Data/clock input voltage level differential peak to peak	0.50	1.0	1.8	
Vindc	DC input voltage (with DC-coupled input) ⁽²⁾	-0.75	0	0.25	V
VQH	Data output voltage amplitude high	-0.05	0	0	V
VQL	Data output voltage amplitude low	-0.95	-0.9	-0.85	V
Tr	Output rise time (20% - 80%)		27		ps
Tf	Output fall time (20% - 80%)		24		ps
Tdl	Input to data output delay ⁽³⁾	125	135	145	ps
FMAx	Clock frequency As a clock divider ⁽⁴⁾	0	12.5	14	GHz

1. Electrical characteristics at ambient temperature.
 2. In case of single-ended inputs, the unused ones must be tied to Vindc which must be set close to the mean value of the used one.
 3. Output change state on input rising edge.
 4. Duty cycle 50%.
 Asymmetrical duty cycle may reduce maximum toggling frequency. 25 Gb/s input working data rate is possible tolerating additional jitter degradations.

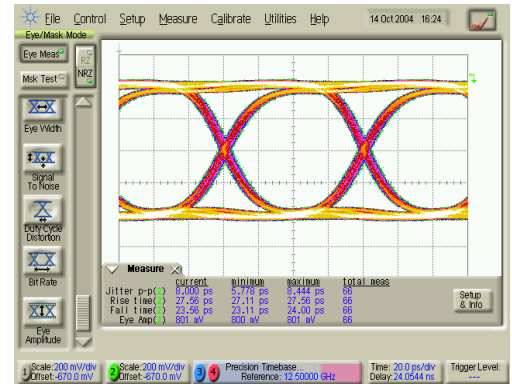
Electrical Characteristics (cont.)

Symbol	Parameters	Min	Typ	Max	Units
RMax	Input data rate ⁽⁴⁾	0	12.5	20 (-25)	Gb/s
RLin	Minimum input return loss (up to 15 GHz)		20		dB
RLout	Minimum output return loss (up to 15 GHz)		5.5		dB
MPW	Minimum pulse width		40		ps
Jpp	Peak to peak jitter	7	8	9	ps
Jrms	RMS jitter		1.3		ps
Ic	Power supply current		136		mA
Pd	Power dissipation		0.71		W

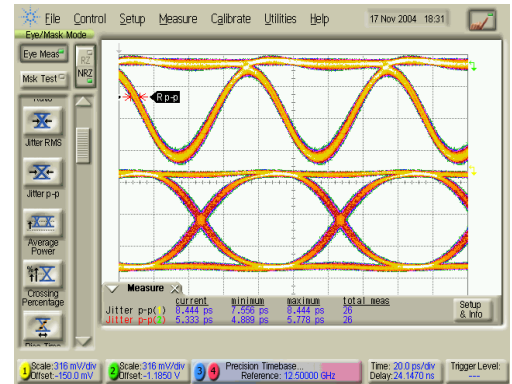
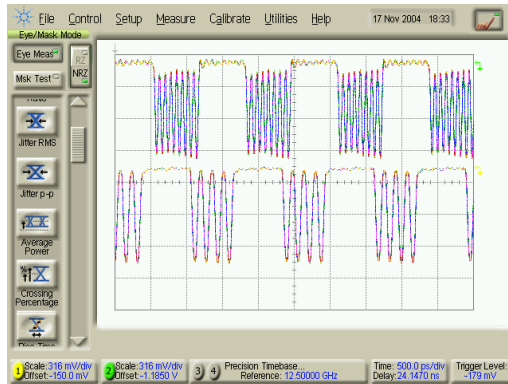
Eye Diagram Performance



Die measurement
 Vee: -5.2 V NRZ input rate: 12.5 Gb/s
 Single-ended data input: +/-250 mVpp

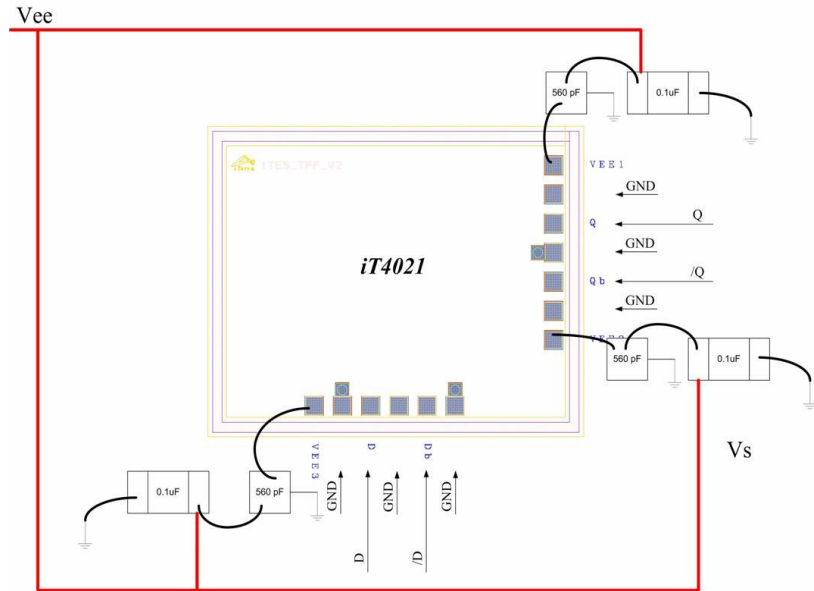


Die measurement
 Vee: -5.2 V + 5% = -4.95 V Clock: 12.5 GHz
 Single-ended data input: +/-450 mVpp



Test board measurement
 VEE: -5.2 V RZ input rate: 12.5 Gb/s (duobinary precoder application)
 Single-ended data input (0,-900 mVpp) DC coupled
 Left: Time domain (fixed pattern) Right: Eye diagram (PN pattern)
 Upper signal: RZ input Lower signal: Duobinary precoded output
 For duobinary use TFF in single-ended input and tune Vindc on unused input.

Recommended Chip Mounting



Pad Positions and Chip Dimensions

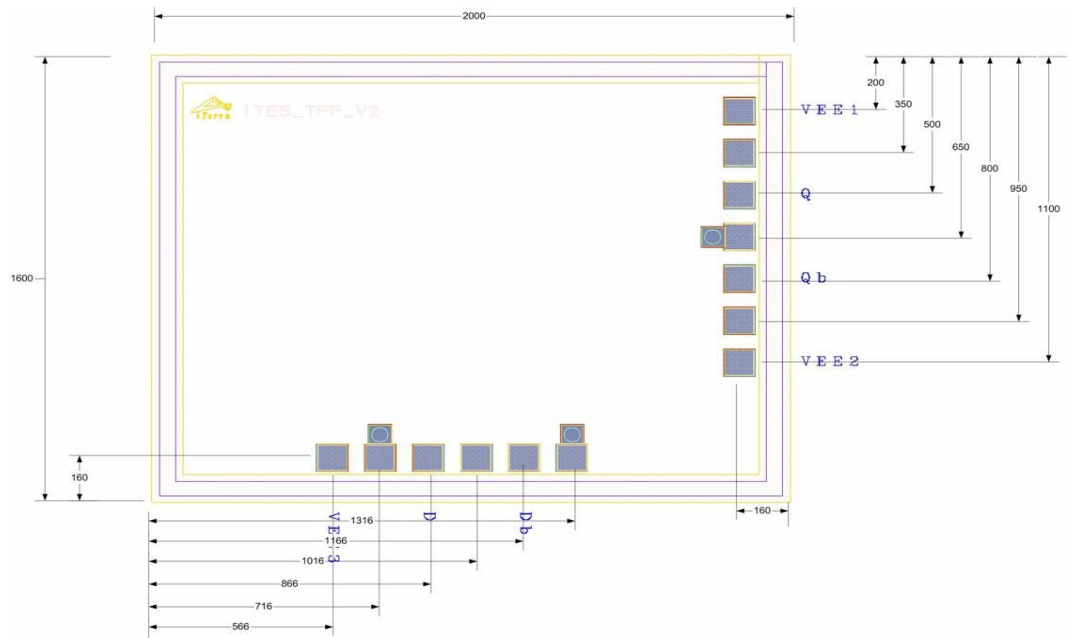
Chip size:
1600 μm ±10 μm x
2000 μm ±10 μm edge
to edge

Chip thickness:
104 μm ±3 μm

Pad size:
100 μm x 100 μm

RF pad pitch:
150 μm

Unlabeled pads are
ground and may be
left floating



Disclaimer

DIGIMIMIC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. DIGIMIMIC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.



DM4021

20 Gb/s (12.5 Gb/s RZ) GaAs MMIC

T-Type Flip-Flop

(Preliminary Information)

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for HBT devices. Note that the backside of the chip is gold plated and it is connected to RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding: for Signal input / output connections, use either 3 mils wide and 0.5 mil thick gold ribbon or a pair of 1mil diameter wires with lengths as short as practical allowing for appropriate stress relief (typically 400 +/- 100 um long). For all other connections, a single 1 mil dia wire of appropriate minimum length may be used.

Product Status Definitions

Datasheet Identification	Product Status	Definition
Advanced Information	Formative or or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. DIGIMIMIC reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not in Production	This datasheet contains specifications on a product that has been discontinued by DIGIMIMIC. The datasheet is printed for reference information only.